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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/752,304	12/28/2000	Thierry D. Besson	M-7928 US	4883

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EXAMINER	
CHAVIS, JOHN Q	
ART UNIT	**PAPER NUMBER**
2124	

DATE MAILED: 07/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/752,304	BESSON, THIERRY D.	
	Examiner	Art Unit	
	John Chavis	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12-28-2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Specification

1. The abstract of the disclosure is objected to because missing items exists for example on page 1, lines 10. The items listed as " XXX" and " YYY" must be corrected or deleted. Correction is required. See MPEP § 608.01(b).

Furthermore, the applicant is hereby advised that website addresses are not allowed to provide support for the specifications. Therefore, every occurrence must be deleted and specific information required for support of the application should be provided. For example, one occurrence exist on line 6 of page 4. Other occurrences exists; however, the applicant should check the entire specification to ensure deletion of all occurrences.

35 USC 102 Rejection

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4, and 7-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Narayan et al.

CLAIMS:	Narayan et al.
1. A method of describing a to-be-built integrated circuit, the method comprising:	See the abstract, which indicates that the system provides for efficient construction (to-be built) of large circuits via Boolean functions (i.e. describing).
reading first data from memory, wherein the first data corresponds to a first cell of a plurality of cells in a library used in manufacturing said integrated circuit,	See section 4.1, which provides for the reading of data corresponding to variables f and g. See also the second paragraph of section 3.2.1, which indicates that data
wherein the first data comprises a plurality of names of a corresponding plurality of signals input to the first cell;	See the introduction, specifically the first paragraph, which refers to a compact representative for Boolean functions (plurality of signals).
and replacing each name in the first data with one of a plurality of new names, respectively, thereby to obtain first renamed data.	This feature is considered inherent to solve various cad problems and to reduce space requirements for ROBDD' s, see paragraphs 2 and 3 of section 1.
2. The method of claim 1 further comprising passing the first renamed data to a predetermined function for	See the abstract, which refers to constructing large circuits (models).

generating at least a first model for said first cell.

3. The method of claim 2 further comprising relating an address in a cell library of the first cell with the first model obtained after said passing.

This feature is considered inherent in claim 2 to enable replacing to occur.

4. The method of claim 3 wherein said first model has a field, and the act of relating comprises: storing said address in said field.

See the referenced portions above.

7. The method of claim 1 further comprising: repeatedly replacing each of the names in the first data with one of the plurality of new names, respectively, in an order different from a previous order used in a previous act of replacing; and

repeatedly passing renamed data obtained from said act of repeatedly replacing to said predetermined function.

See the rejection of claim 6.

8. The method of claim 1 further comprising: reading second data from memory, wherein the second data corresponds to a second cell of the

See again the rejection of claim 6.

plurality of cells, wherein the second data comprises a plurality of names of a corresponding a plurality of signals input to the second cell; and

replacing each name in the second data with one of new names, respectively, thereby to obtain second renamed data.

9. The method of claim 8 further comprising: passing the first renamed data to a predetermined function for generating first BDD or ROBDD data;

passing the second renamed data to said predetermined function for generating second BDD or ROBDD data;

relating an address of the first cell to the first BDD or ROBDD data; and relating an address of the second cell to the second BDD or ROBDD data.

See the rejection of claim 6.

10. The method of claim 1 further comprising: reading second data from memory, wherein the second data corresponds to a portion of a network to-be-built of interconnected circuits, wherein the second data comprises a

See again the rejection of claim 6.

plurality of names representing a plurality of signals input to the portion;

and replacing each name of the second data with one of a plurality of new names, respectively, thereby to obtain second renamed data.

In reference to claims 11-12, and 16-19, see the rejection of claim 10 and the first paragraph of section 2. The tree structure in section 3.2.1 provides for the data structure and table features.

The storage medium of claim 13 is inherent to enable stored data to be retrieved and to enable data to be replaced.

As per the signal carrier of claim 14, see fig. 1.

In reference to claim 15, 20-23, see the rejection of claim 1.

35 USC 103 Rejection

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narayan et al. in view of the applicant's choice of utilizing a different order for replacing names.

Claims	Narayan
5. The method of claim 1 wherein after said replacing, the method further comprises replacing each of the names in the first data with one of the plurality of new names, respectively, in a second order different from a first order of said new names used to obtain the first renamed data, thereby to obtain second renamed data.	The order of replacing names is considered a choice of design; since, the overall functionality remains the same in that one name is merely replaced with another.
6. The method of claim 5 further comprising: passing the first renamed data to a predetermined function for generating first model; passing the second renamed data to said predetermined function for generating second model; relating an address of the first cell to the	These features are considered taught by the plurality of data referenced in claim 1.

first model; and

relating said address to the second model.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Chavis whose telephone number is (703) 305-9665. The examiner can normally be reached on 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jqc
June 28, 2004

JOHN CHAVIS
PATENT EXAMINER
ART UNIT 2124